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PHASE-PULSE MULTISTABLE COUNTING CIRCUIT,(U)
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FOREIGN TECHNOLOGY DIVISION

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PHASE-PULSE MULTISTABLE COUNTING CIRCUIT

by

L.A. Dubitskiy

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EDITED TRANSLATION

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PHASE-PULSE MULTISTABLE COUNTING CIRCUIT

By: L.A. Dubitskiy

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U. S. BOARD ON GEOGRAPHIC NAMES TRANSLITERATION SYSTEM

Block	Italic	Transliteration	Block	Italic	Transliteration
А а	*А а*	A, a	Р р	*Р р*	R, r
Б б	*Б б*	B, b	С с	*С с*	S, s
В в	*В в*	V, v	Т т	*Т т*	T, t
Г г	*Г г*	G, g	У у	*У у*	U, u
Д д	*Д д*	D, d	Ф ф	*Ф ф*	F, f
Е е	*Е е*	Ye, ye; E, e*	Х х	*Х х*	Kh, kh
Ж ж	*Ж ж*	Zh, zh	Ц ц	*Ц ц*	Ts, ts
З з	*З з*	Z, z	Ч ч	*Ч ч*	Ch, ch
И и	*И и*	I, i	Ш ш	*Ш ш*	Sh, sh
Й й	*Й й*	Y, y	Щ щ	*Щ щ*	Shch, shch
К к	*К к*	K, k	Ъ ъ	*Ъ ъ*	"
Л л	*Л л*	L, l	Ы ы	*Ы ы*	Y, y
М м	*М м*	M, m	Ь ь	*Ь ь*	'
Н н	*Н н*	N, n	Э э	*Э э*	E, e
О о	*О о*	O, o	Ю ю	*Ю ю*	Yu, yu
П п	*П п*	P, p	Я я	*Я я*	Ya, ya

*ye initially, after vowels, and after ъ, ь; e elsewhere.
When written as ё in Russian, transliterate as yё or ё.

RUSSIAN AND ENGLISH TRIGONOMETRIC FUNCTIONS

Russian	English	Russian	English	Russian	English
sin	sin	sh	sinh	arc sh	$\sinh^{-1}$
cos	cos	ch	cosh	arc ch	$\cosh^{-1}$
tg	tan	th	tanh	arc th	$\tanh^{-1}$
ctg	cot	cth	coth	arc cth	$\coth^{-1}$
sec	sec	sch	sech	arc sch	sech^{-1}
cosec	csc	csch	csch	arc csch	csch^{-1}

Russian	English
rot	curl
lg	log

0185,gw

PHASE-PULSE MULTISTABLE COUNTING CIRCUIT

L. A. Dubitskiy.

The invention relates to the area of computer technology and is intended for counting the number of pulses and the division of the pulse repetition frequency. It may be used in particular in electronic counting frequency meters. Phase-pulsed multistable counting circuits containing a storage capacitor and a self-tuning capacitor have found wide application.

However, such devices are characterized by a small range of permissible changes of the comparison voltage when comparing the voltages on the self-tuning- and storage capacitors which reduces the reliability of the device as a whole. This is connected with the fact that the change in the comparison voltage leads to a change of ampltude of the discharge pulse of the self-tuning capacitor, the amplitude of this pulse is equal to the difference between the amplitude of the reset pulses and the comparison voltage.

In known counters the value of the amplitude of the reset pulses and the comparison voltage are close which leads to a strong dependence of the pulse amplitude of the discharge of the self-tuning capacitor on the comparison voltage.

The described device makes it possible to expand the range of measurements of the comparison voltage, and to raise the operational reliability of the device.

This is achieved due to the use, for discharge of the self-tuning capacitor, of pulses the amplitude of which significantly exceeds the comparison voltage.

The drawing shows a schematic of the device.

It consists of an input amplifier-limiter 1; a linearizing cascade with a storage cell 2; a gate 3; a comparator 4; a self-tuning capacitor 5; a reset circuit 6; a voltage amplifier 7; a discharge circuit of the self-tuning capacitor 8, the control input of which is connected to the output of amplifier 7; the potential input - to the supply bus, and the output, to the self-tuning capacitor 5. Capacitor 5 is connected by one plate with the output of

the comparator 4 and by the other with the input of circuit 6, the ouput of which is connected to the input of amplifier 7. The ouput of amplifier 7, through gate 3, is connected to the linearizing cascade with storage cell 2, which is connected by the input with the output of the amplifier-limiter 1.

The operation of the device proceeds in the following manner.

A train of pulses, removed from the amplifier-limiter 1, is stored by the storage cell 2 in the form of an increasing staircase voltage. During comparison, in comparator 4, of this voltage with the voltage recorded earlier on capacitor 5 a reset pulse enters the input of circuit 6. Circuit 6 forms the pulse which is amplified with respect to voltage by amplifier 7 and through gate 3 discharges storage cell 2. Subsequently the cycle is repeated. The pulse present at the output of amplifier 7 is not only a reset pulse and an output pulse but also monitors the discharge of the self-tuning capacitor 5. After each subsequent comparison the excess charge enters capacitor 5. This charge is determined by the ratio of voltages stored in storage cell 2 and capacitor 5. This charge leads to an increase in the voltage on the self-tuning capacitor and the following comparison may bring about changes of the division coefficient of the divider. Therefore, for maintaining the assigned division coefficient the self-tuning capacitor 5 must be discharged after each subsequent

comparison. This is achieved by the action of a reset pulse through the discharge circuit 8 of the self-tuning capacitor. Circuit 8 monitors the quantity of charge drawn off from capacitor 5 as a result of which frequency-independent self-tuning is achieved.

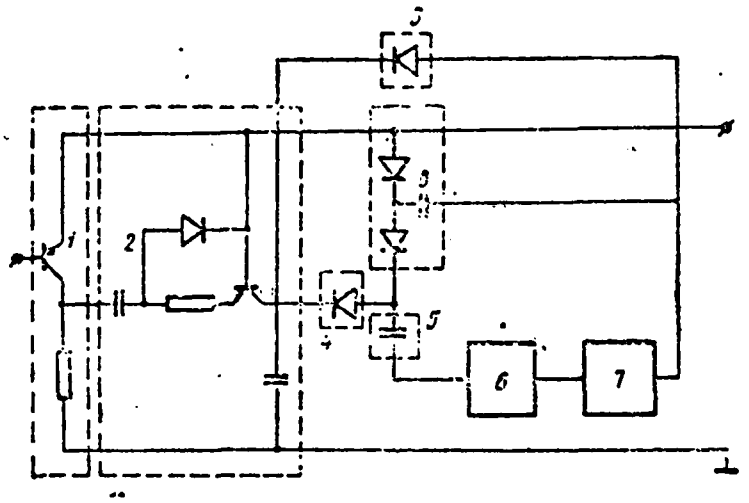
The amplitude of pulses arriving from voltage amplifier 7 to discharge circuit 8 significantly exceeds the voltage stored on self-tuning capacitor 5 (comparison voltage). This means that a change of the comparison voltage has little effect on the amplitude of pulses discharging capacitor 5 and consequently on the position of the level of comparison. Thus, pulses arriving at reset circuit 6 depend little on the comparison voltage.

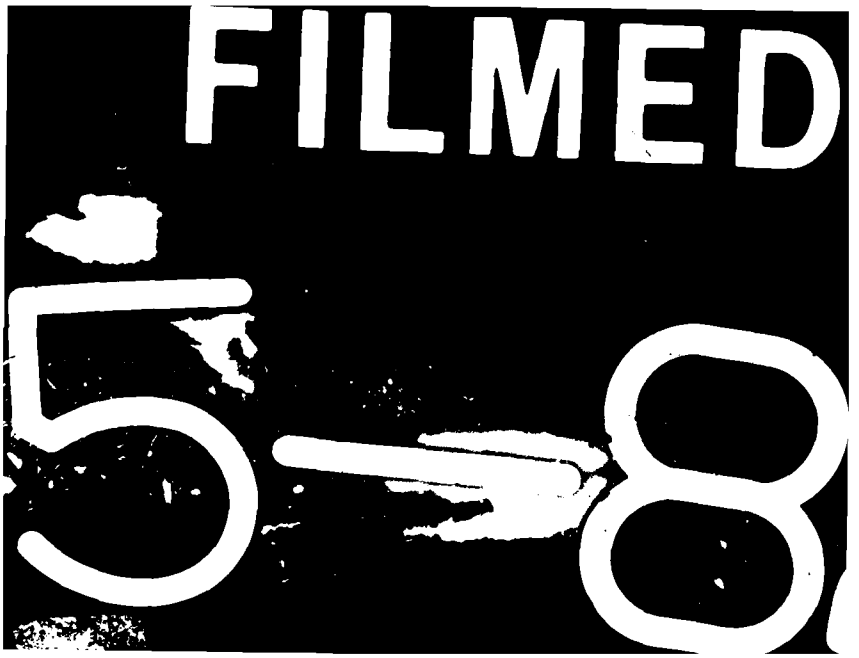
The range of change of the comparison voltage is expanded, considerably increasing the operational reliability of the device.

Object of Invention.

Phase-pulse multi-stable counting circuit containing an input amplifier-limiter connected to a linearizing cascade with a storage cell, the output of which is connected with a comparator, to the second input of which is connected a self-tuning capacitor, and the output of the comparator is connected with a reset circuit which is connected to the discharge circuit of the self-tuning capacitor and

to the gate connected with the storage cell, is distinguished by the fact that for the purpose of increasing the reliability of counting it contains a voltage amplifier, whereby the input of the amplifier is connected with the output of the reset circuit and the output, with the input of the discharge circuit of the self-tuning capacitor.

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